CLAIM LISTING

This listing of claims will replace all prior versions and listings of claims in the application:

IN THE CLAIMS

1. (Currently Amended) A method for processing data within a programmable gate array, the method comprises:

detecting, by a fixed logic processor embedded within the programmable gate array, a custom operational code;

providing, by the fixed logic processor, an indication of the custom operational code to the programmable gate array in response to detecting the custom operational code; and

performing, by at least a portion of the programmable gate array configured as a dedicated processor, a fixed logic routine in response to receiving the indication of the custom operational code,

wherein the providing the indication of the custom operational code further comprises at least one of:

providing data for processing to a portion of the programmable gate array;

providing a co-processing instruction to the at least a portion of the programmable gate array, wherein the co-processing instruction indicates co-processing of the data;

providing a second co-processing instruction to the at least a portion of the programmable gate array, wherein the second co-processing instruction indicates fetching second data for co-processing;

providing an interrupt instruction to the at least a portion of the programmable gate array, wherein the interrupt instruction indicates interrupt processing of the data;

providing a second interrupt instruction to the at least a portion of the programmable gate array, wherein the second interrupt instruction indicates fetching the second data for interrupt processing; and

providing a system management instruction to the at least a portion of the programmable gate array.

2. (Original) The method of claim 1, wherein the detecting the custom operational code further comprises:

executing, by the fixed logic processor, an algorithm that includes a series of instructions from a standard instruction set, wherein the standard instruction set corresponds to an architecture of the fixed logic processor; and

detecting, while executing the algorithm, the custom operational code.

3. (Cancelled)

4. (Original) The method of claim 1, wherein the providing the custom operational code further comprises:

providing the custom operational code to the at least a portion of the programmable gate array via an auxiliary processing interface of the fixed logic processor.

5. (Original) The method of claim 1 further comprises:

generating, by the at least a portion of the programmable gate array, processed data as a result of performing the fixed logic routine; and

providing, by the at least a portion of the programmable gate array, the processed data to the fixed logic processor.

6. (Original) The method of claim 5, wherein the providing the processed data further comprises at least one of:

receiving, from the fixed logic processor, a request for providing the processed data, wherein the request is received in response to providing a data ready indication by the at least a portion of the programmable gate array to the fixed logic processor;

providing, by the at least a portion of the programmable gate array, the processed data to the fixed logic processor upon completion of performing the fixed logic routine; and

receiving, from the fixed logic processor, a request for providing the processed data, wherein the request is received in response to the fixed logic processor monitoring the performing of the fixed logic routine.

7. (Original) The method of claim 1 further comprises:

pre-configuring the at least a portion of the programmable gate array to perform the fixed logic routine.

8. (Original) The method of claim 1 further comprises:

detecting, by the fixed logic processor embedded within the programmable gate array, a second custom operational code;

providing, by the fixed logic processor, an indication of the second custom operational code to the programmable gate array in response to detecting the second custom operational code; and

performing, by a second portion of the programmable gate array configured as a second co-processor, a second fixed logic routine in response to receiving the indication of the second custom operational code.

9. (Original) The method of claim 1 further comprises:

detecting, by a second fixed logic processor embedded within the programmable gate array, the custom operational code;

providing, by the second fixed logic processor, the indication of the custom operational code to the programmable gate array in response to detecting the custom operational code; and

performing, by at least the portion of the programmable gate array configured as a co-processor, the fixed logic routine in response to receiving the indication of the custom operational code.

10. (Original) The method of claim 1 further comprises:

detecting, by a second fixed logic processor embedded within the programmable gate array, a second custom operational code;

providing, by the second fixed logic processor, an indication of the second custom operational code to the programmable gate array in response to detecting the second custom operational code; and

performing, by a second portion of the programmable gate array configured as a second co-processor, a second fixed logic routine in response to receiving the indication of the second custom operational code.

11-22. (Cancelled)

23. (Currently Amended) A programmable gate array comprises:

logic fabric that includes a plurality of configurable logic blocks, switching blocks, and input/output blocks;

fixed logic processor embedded within the logic fabric; and

memory operably associated with the fixed logic processor and the logic fabric, wherein, based on operational instructions stored in memory, the fixed logic processor:

detects a custom operational code;

provides an indication of the custom operational code to the logic fabric in response to detecting the custom operational code; and

wherein, based on further operational instructions stored in the memory, at least a portion of the logic fabric: performs a fixed logic routine in response to receiving the indication of the custom operational code,

wherein the memory further comprises operational instructions that cause the fixed logic processor to provide the indication of the custom operational code by at least one of:

providing data for processing by the at a portion of the logic fabric;

providing a co-processing instruction to at least a portion of the logic fabric, wherein the co-processing instruction indicates co-processing of the data;

providing a second co-processing instruction to at least a portion of the logic fabric, wherein the second co-processing instruction indicates fetching second data for co-processing;

providing an interrupt instruction to the at least a portion of the logic fabric, wherein the interrupt instruction indicates interrupt processing of the data;

providing a second interrupt instruction to the at least a portion of the programmable gate array, wherein the second interrupt instruction indicates fetching the second data for interrupt processing; and

providing a system management instruction to the at least a portion of the logic fabric.

24. (Original) The programmable gate array of claim 23, wherein the memory further comprises operational instructions that cause the fixed logic processor to detect the custom operational code by:

executing an algorithm that includes a series of instructions from a standard instruction set, wherein the standard instruction set correspond to an architecture of the fixed logic processor; and

detecting, while executing the algorithm, the custom operational code.

25. (Cancelled)

26. (Original) The programmable gate array of claim 23, wherein the memory further comprises operational instructions that cause the fixed logic processor to provide the custom operational code by:

providing the custom operational code to the at least a portion of the logic fabric via an auxiliary processing interface of the fixed logic processor.

27. (Original) The programmable gate array of claim 23, wherein the memory further comprises operational instructions that cause the at least a portion of the logic fabric to:

generate processed data as a result of performing the fixed logic routine; and

provide the processed data to the fixed logic processor.

28. (Original) The programmable gate array of claim 23, wherein the memory further comprises operational instructions that cause the at least a portion of the logic fabric to provide the processed data by at least one of:

receiving, from the fixed logic processor, a request for providing the processed data, wherein the request is received in response to providing a data ready indication by the at least a portion of the logic fabric to the fixed logic processor;

providing the processed data to the fixed logic processor upon completion of performing the fixed logic routine; and

receiving, from the fixed logic processor, a request for providing the processed data, wherein the request is received in response to the fixed logic processor monitoring the performing of the fixed logic routine.

29. (Original) The programmable gate array of claim 23, wherein the memory further comprises operational instructions that cause the fixed logic processor to:

detect a second custom operational code;

provide an indication of the second custom operational code to the logic fabric in response to detecting the second custom operational code; and

wherein, based on further operational instructions stored in the memory, a second portion of the logic fabric performs a second fixed logic routine in response to receiving the indication of the second custom operational code.

30. (Original) The programmable gate array of claim 23 further comprises:

a second fixed logic processor, wherein the memory further comprises operational instructions that cause the second fixed logic processor to:

detect the custom operational code;

provide the indication of the custom operational code to the programmable gate array in response to detecting the custom operational code; and

wherein, based on the further operational instructions stored in the memory, the at least a portion of the logic fabric:

performs the fixed logic routine in response to receiving the indication of the custom operational code.

31. (Original) The programmable gate array of claim 23 further comprises:

a second fixed logic processor, wherein the memory further comprises operational instructions that cause the second fixed logic processor to:

detect a second custom operational code;

provide an indication of the second custom operational code to the logic fabric in response to detecting the second custom operational code; and

wherein, based on further operational instructions stored in the memory, a second portion of the logic fabric performs a second fixed logic routine in response to receiving the indication of the second custom operational code.

32-43. (Cancelled)

RESPECTFULLY SUBMITTED,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on November 5, 2004.

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